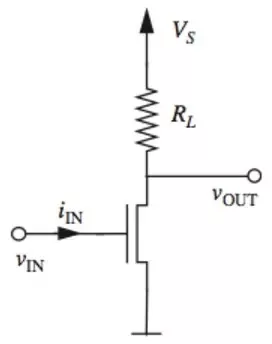
**DIGITAL CIRCUIT AND SYSTEMS**

**ASSIGNMENT 3**

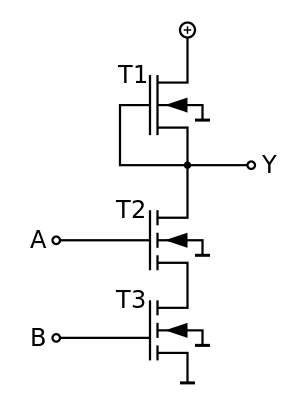
SUBMITTED BY: Manan Madan (2018UIC3087)

**Q1. NMOS LOGIC**

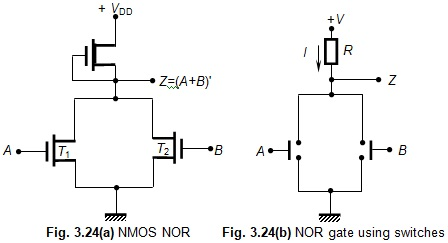
1. NOT GATE



1. NAND GATE (DEPLETION TYPE)

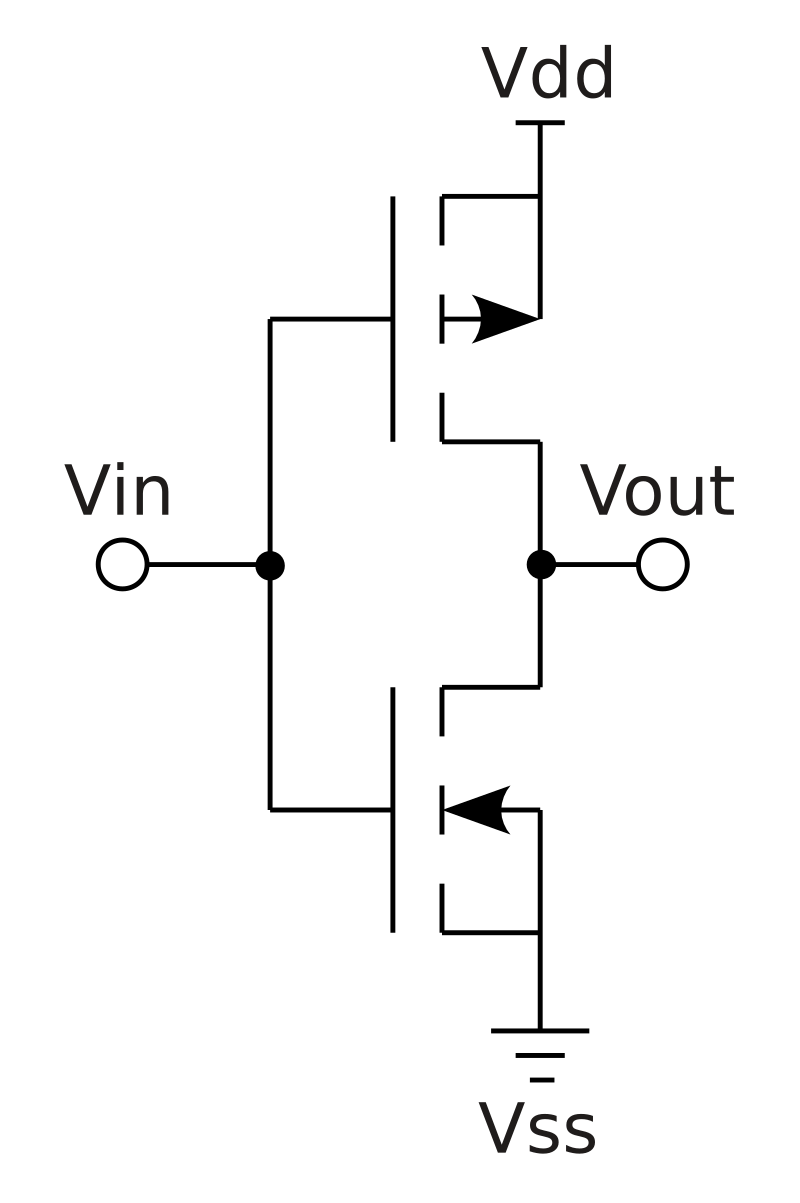


1. NOR GATE

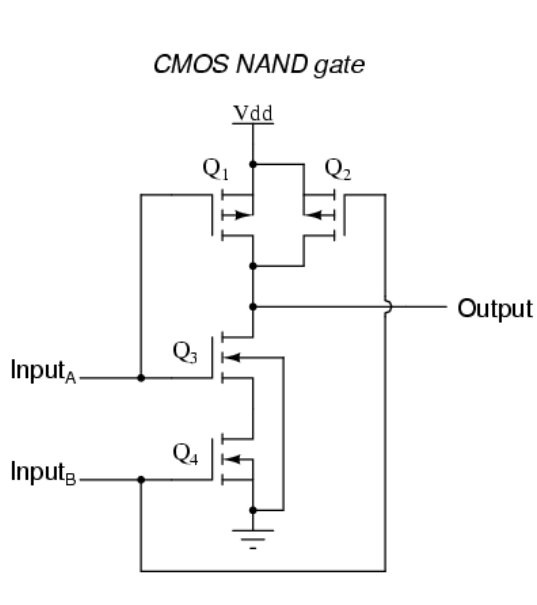


**Q2. CMOS LOGIC**

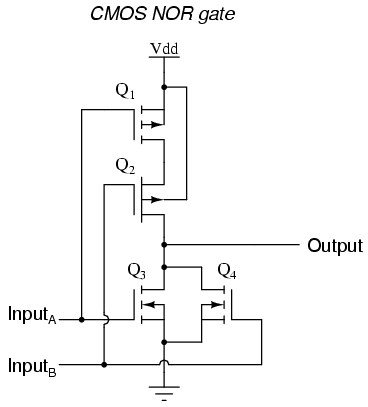
1. NOT GATE



1. NAND GATE



1. NOR GATE



**Q3. SHORT NOTE ON CMOS TRANSMISSION GATE**

The transmission gate is a [CMOS](https://en.wikipedia.org/wiki/CMOS)-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both [PMOS](https://en.wikipedia.org/wiki/PMOS_logic) and [NMOS](https://en.wikipedia.org/wiki/NMOS_logic) work simultaneously.

It is constructed using two [field-effect transistors](https://en.wikipedia.org/wiki/Field-effect_transistors), in which the substrate terminal (bulk) is not connected internally to the source terminal.

The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate ([inverter](https://en.wikipedia.org/wiki/Inverter_(logic_gate))), to form the control terminal.

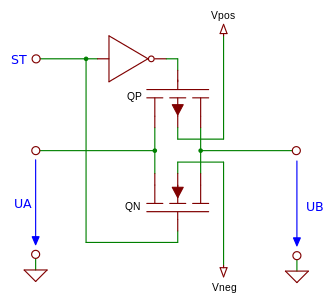


Fig: Schematic diagram

**Functioning**

When the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off.

When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start conducting at a voltage difference between the gate terminal and one of these conducts.

One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the n-channel MOSFET, and this begins to turn off. At the same time, the p-channel MOSFET has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches.

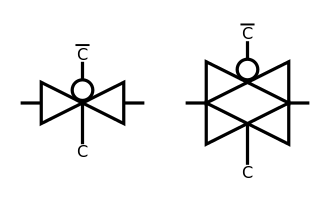


Fig: Traditional symbols

|  |  |
| --- | --- |
| **CONTROL** | **Switch** |
| 0 V | Open (OFF) |
| +Vdd | Closed (ON) |

*Where Vdd is potential difference between Vp and Vn*

Fig: Functional Table